REMARKS

This Amendment is responsive to the Final Office Action dated October 22, 2004. All objections and rejections of the Examiner are respectfully traversed. Reconsideration and further examination is respectfully requested.

In paragraphs 2-14 the Examiner rejected claims 1-33 for obviousness under 35 U.S.C. 103, citing the combination of United States patent number 6,438,141 of Hanko et al. ("Hanko et al.") and United States patent number 6,598,080 of Nagami et al. ("Nagami et al."), as well as United States patent number 6,687,247 of Wilford et al. ("Wilford et al.") Applicants respectfully traverse this rejection.

As discussed in Applicants' response to the previous rejection based on the combination of Hanko et al. and Nagami et al., Hanko et al. includes a technique for predicting bandwidth requirements that utilizes historical information concerning data rates, and that applies an exponential moving average (EMA) method. The parameters of the EMA method in Hanko et al. may be selected to provide statistical measurements of data rates, such as an approximation of the mean plus one standard deviation on normally distributed streams of data or sets of bandwidth allocations. Hanko et al. teach that their system can be implemented using a computer including a video memory, main memory and mass storage, all coupled to bi-directional system bus, along with keyboard, mouse and processor. The Hanko et al. system bus is described as containing 32 address lines for addressing and also a 32-bit data bus for transferring data. As further described by Hanko et al., a data source may calculate a number of bits or pixels and the period of time over which they will be generated, and divide the number of bits or pixels by the

period of time, to generate a bits per second or pixels per second value. A data source of Hanko et al. statistically combines these values with historical data to produce statistical values, such as a set of values representative of the mean plus one standard deviation of the bits per second and pixels per second values. These statistical values are used by the Hanko et al. system to produce an estimate of bandwidth needs in both bits per second and pixels per second. As also discussed in Applicants' previous response, Nagami et al. disclose a network interconnection system using a control message including information for storing, in a memory of a node, a correspondence relationship between a first virtual path to be used in receiving a packet from a first logical network to a virtual path to be used in transmitting the packet to the other logical network.

The Examiner acknowledges, as argued previously, that the combination of Hanko et al. and Nagami et al. does not disclose or suggest any system or method in which a single memory location of a memory device is used to store statistical value including a packet count and a statistical value including a byte count. It is now asserted that such a feature is disclosed by Wilford et al., and Applicants respectfully disagree with this analysis for the following reasons.

Wilford et al. generally disclose a linecard architecture for high speed routing of data in a communications device. In the Wilford et al. system, low latency routing is provided based on packet priority such that packet routing and processing occurs at line rate (wire speed) for most operations. The packet header alone is used to perform a high speed routing lookup by the Wilford et al. system. Enqueued packets are buffered by Wilford et al. within a large memory space holding multiple packets prior to transmission across a switch fabric to an outbound linecard. On arrival at the outbound linecard, the packet is enqueued by the Wilford et al. system in an outbound transmitter portion of the linecard architecture.

With regard to statistics, Wilford et al. describe a Committed Access Rate (CAR) Statistics Module beginning at line 43 of column 52, as shown receiving data from the Token Bucket Module in Fig. 30. Wilford et al. state as follows in this regard:

> The CAR Statistics Module keeps a count of all packets and bytes passed and dropped per token bucket. The packet ***counters*** are 32 bits and byte ***counters*** 40 bits. The drop ***counters*** will be approximately 4 bits smaller as we should not be dropping at full line rate for very long so packet drop ***counters*** are 28 bits and byte drop counters are 36 bits. All of these ***counters*** should saturate (i.e. not roll over) and clear when read by the CPU.

Wilford et al. include no other discussion of counters. The teaching of Wilford et al. with regard to packet count and byte count statistics is limited to the provision of counters of some kind, without a hint or suggestion as to the specific structure or operation of the counters, beyond suggested sizes, and that the counters should not roll over. Wilford et al. lacks any teaching that would lead one skilled in the art to the feature of the present independent claims in which ***a single memory location of a memory device is used to store statistical value including a packet count and a statistical value including a byte count*** (see claims1, 12 and 23). Wilford et al. includes descriptions of memory for storing received packet data and headers, but not with regard to storing the counters. The mere teaching of a "counter" of some kind in this regard is not sufficient, as shown by the following definition of "counter" from the on-line technical encyclopedia found at www.techweb.com:

> In programming, a variable that is used to keep track of anything that must be counted. The programming language determines the number of counters (variables) that are available to a programmer.

Accordingly, given this ordinary definition of the term "counter", a person skilled in the art, upon reading Wilford et al., even in the context of the teachings of Hanko et al. and Nagami et al., would *not* be guided towards the above set forth feature of the present independent claims 1, 12 and 23.

In conclusion, for the reasons stated above, nowhere in the combination of Hanko et al., Nagami et al. and Wilford et al. is there disclosed or suggested any system or method for monitoring a network, that includes:

. . .

> reading an entry of a memory device, the entry of the memory device containing a first statistical value and a second statistical value, ***wherein the entry is a single memory location of the memory device, wherein the first statistical value includes a packet count, and wherein the second statistical value includes a byte count***;
>
> determining a third statistical value based on at least one of a content of the at least one data packet, the first statistical value, and the second statistical value; and
>
> storing the determined third statistical value in the entry of the memory device. (emphasis added)

as in the present independent claims 1, 12 and 23. The combined references provide any hint or suggestion of even the desirability of providing any system or method that includes *storing packet count and byte in a single memory location, such that another statistical value is determined based on the content of a received data packet, and is then written to that single memory location*, as in the present independent claims 1, 12 and 23.

For the above reasons, Applicants respectfully urge that the combination of Hanko et al., Nagami et al. and Wilford et al. fails to disclose or suggest all the features of the present independent claims 1, 12 and 23. Accordingly, the combination of Hanko et al., Nagami et al. and Wilford et al. does not support a *prima facie* case of obviousness with regard to the present independent claims 1, 12 and 23 under 35 U.S.C. 103. As to the remaining claims, they each

depend either directly or indirectly from independent claims 1, 12 and 23, and are respectfully believed to be patentable over the combination of Hanko et al., Nagami et al. and Wilford et al. for at least the same reasons. Reconsideration of all pending claims is respectfully requested.

In view of the above, Applicants respectfully urge that the present claims are allowable, and request that the rejections of the Final Office Action be withdrawn.

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone David A. Dagg, Applicants' Attorney at 978-264-6664 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

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Date

David A. Dagg Reg. No. 37,809
Attorney/Agent for Applicant(s)
Steubing McGuinness & Manaras LLP
125 Nagog Park Drive
Acton, MA 01720
(978) 264-6664

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